

MetaEmu

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METAEMU: An Architecture Agnostic Rehosting Framework for Automotive Firmware

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ABSTRACT

In this paper we present METAEMU, an architecture-agnostic framework geared towards rehosting and security analysis of automotive firmware. METAEMU improves over existing rehosting environments in two ways: Firstly, it solves the hitherto open-problem of a lack of generic Virtual Execution Environments (VXEs) by synthesizing processor simulators from Ghidra’s language definitions. Secondly, METAEMU can rehost and analyze multiple targets, each of different architecture, simultaneously, and share analysis facts between each target’s analysis environment, a technique we call inter-device analysis.

We show that the flexibility afforded by our approach does not lead to a performance trade-off—METAEMU lifts rehosted firmware to an optimized intermediate representation, and provides performance comparable to existing emulation tools, such as Unicorn. Our evaluation spans five different architectures, bare-metal and RTOS-based firmware, and three kinds of automotive Electronic Control Unit (ECU) from four distinct vendors—none of which can be rehosted or emulated by current tools, due to lack of processor support. Further, we show how METAEMU enables a diverse set of analyses by implementing a fuzzer, a symbolic executor for solving peripheral access checks, a CAN ID reverse engineering tool, and an inter-device coverage tracker.

KEYWORDS

automotive; dynamic program analysis; firmware; emulation

1 INTRODUCTION

Automobiles fulfill a vital function in our societies—a means of transport—and, as with many technologies, have become increasingly connected, and at the same time more closed to scrutiny [33]. Kocher et al. [31] and Checkoway et al. [6] demonstrated that this increased connectivity introduces a significant attack surface, and, inspired by these seminal works, Miller and Valasek [39] showed that automobiles, like any other Internet-connected device can be remotely compromised. Meanwhile, Garcia et al. [21] and Verdult et al. [53, 54] showed that physical entry to a vehicle—something traditionally handled by a mechanical means—could also be defeated.

While researchers have sought to mitigate these flaws by protocol enhancements, e.g., [4], analyzing the black-box firmware of the ECUs connected to a vehicle’s internal network, has largely been left as a manual endeavor, e.g., [14]. We posit that this is due to the fact that, while ECU firmware is not necessarily hard to obtain, tool support for performing anything more than manual analysis is severely lacking for the processor architectures they are based on.

Recent approaches enabling security analysis of embedded devices have primarily focused on rehosting, i.e., the process of transplanting a device’s firmware to run inside a virtualized execution environment, e.g., QEMU [3] or derived tools, such as Unicorn [46], to enable specific analysis tasks. While these environments support a wide-range of commonly used embedded architectures, such as ARM and MIPS, they do not provide out-of-the-box support for arbitrary peripherals, or any support for esoteric architectures, such as those found in automotive components. At the time of writing, most published work has sought to address the former challenge: peripheral support. However, as noted by Fasano et al. [17] in their systematization of the field, for devices whose firmware is not supported by an off-the-shelf emulator, the latter challenge—obtaining a suitable execution environment—remains an open problem, hampering the analysis of a large and vital class of devices.

An orthogonal issue arising from the use of commodity emulators for rehosting is that they implicitly force a device-centric approach, where a device and its peripherals are assumed to operate with little or no constraints on the inputs they receive. For many scenarios where embedded devices are deployed, we believe that this simplification is unjustified, as evidenced in recent work by industry practitioners [51, 52]. In the automotive setting, for example, ECUs are interconnected by a Controller Area Network (CAN) bus, which they use to communicate. Many ECUs require the presence of other ECUs to successfully initialize and operate, hence, to realistically simulate a device’s operating environment, we often require more than a single ECU to be rehosted.

Our contribution In this paper, we address the challenge of analyzing devices that cannot be rehosted using commodity emulators. We present our framework, METAEMU, that takes as input widely available processor and instruction set definitions—Ghidra’s language definitions, and automatically synthesizes virtualized execution environments capable of rehosting multiple devices of different architectures simultaneously. Our synthesized environments enable deep introspection of each rehosted firmware’s state and facilitate complex inter-device analyses.

We demonstrate that our approach is general (it can support rehosting firmware of many architectures, irrespective of their peculiarities), scalable (it can analyze many instances of a firmware in parallel and share analysis facts), and enables dynamic analysis of devices that until now have been largely overlooked.

To evaluate METAEMU, we benchmark its performance and provide six case studies detailing its use for different kinds of security analysis, including backdoor detection, inter-device analysis, and various automotive-focused reverse engineering tasks. For these analyses, we implement a fuzzer (by integrating METAEMU with LibAFL [20]), a symbolic executor, which we use to solve peripheral access checks, a CAN bus reverse-engineering tool, and an

*Both authors contributed equally to this research.

inter-firmware coverage tracker. Our case studies demonstrate that METAEMU is effective in analyzing complex, binary-only firmware, without any architecture support or performance trade-off. Our evaluation data-set consists of thirteen benchmarks and six device firmware: two based on open-source SDKs and four extracted from automotive ECUs: a Body Control Module (BCM), an Instrument Cluster (IC), and two Telematics Control Units (TCUs). Each end-user firmware is based on a different CPU architecture (Infineon C166 and Renesas RH850, SH-2A, and V850E2M-M), and each presents a different set of challenges for emulation and analysis.

To summarize, our work makes the following contributions:

- (1) We present, to the best of our knowledge, the first generic framework for rehosting and dynamically analyzing end-user automotive firmware, and the first framework supporting device inter-dependent analysis of multiple rehosted firmware executing simultaneously.
- (2) We show that our framework is capable of synthesizing VXEs for multiple esoteric architectures, generically enabling analysis of a vital class of devices currently unsupported by any other dynamic analysis framework.
- (3) We show how our framework enables complex analyses, such as symbolic execution and fuzz testing, to be applied to binary-only automotive firmware.
- (4) We provide an in-depth evaluation of METAEMU, with respect to performance, implementation flexibility, and real-world usability. It spans five different architectures, bare-metal and RTOS-based firmware, and three kinds of automotive ECU from four distinct vendors.

We release our framework, processor definitions, and firmware data-set as open-source [7].

2 BACKGROUND

In this section, we provide the necessary background to understand our contributions. We first provide an overview of the challenges involved in analyzing automotive components, and then cover the terminology used in the rest of this article.

A modern vehicle is composed of multiple ECUs connected by a CAN bus. Each ECU may have multiple peripherals, and often, each will be manufactured by a different vendor, and may be based on a different CPU architecture. In contrast to the majority of devices analyzed under the umbrella of “embedded device security” in the literature, ECUs are generally based on more esoteric architectures, e.g., V850/RH850, or C166, rather than ARM or MIPS. Unfortunately, these architectures are not supported at all by the de facto emulation environments for security analysis—QEMU and Unicorn. This makes it impossible to apply modern security analysis approaches such as symbolic execution to these devices. While one might assume that this challenge can be addressed by adding support for new architectures to those tools, doing so requires an unreasonably large amount of engineering effort: 1000s of lines of code and many months of development time—an unjustifiable amount of work for most applications. While Ghidra has EmulatorHelper which can be used to emulate some of these architectures, it does not have an easy-to-use interface for peripheral handling or adequate performance for intensive analyses.

The tangential problem of peripheral support is a significant challenge in the automotive context: on the one hand, due to the variety and number of peripherals a single firmware might interface with, and on the other, due to a lack of documentation. For some analysis tasks, peripheral interactions can be *bypassed* by providing a satisfying value which will work even with limited information about the peripheral, as is done in previous work [5, 19, 60]. However, such a bypass is often no better than (unsoundly) forcing execution of a given branch target. This is because the *real* constraints on the peripheral register might depend on another device’s output, or be constrained outside the execution path being analyzed. An obvious example of such a peripheral is a Compare and Match Timer (CMT), which is often used by firmware to implement task scheduling. Clearly, providing *any* satisfying value for the peripheral’s output will lead to undesired behavior, and is better handled by a modeling approach, such as that proposed by Gustafson et al. [24]. Thus, support for peripheral models and the ability to have multiple rehosted firmware interact and communicate is vital to ensure faithful simulation.

METAEMU provides a means to rehost one or more device firmware inside a virtual execution environment. We use the term *rehost* to jointly refer to the process of transplanting a device’s firmware into an emulator, and the simulation of its execution and interaction with its peripherals. In this work, we refer to the rehosting environment as a VXE, and assume that a VXE facilitates multiple firmware to coexist and interact with each other. METAEMU synthesizes VXEs; we distinguish a synthesized VXE from a standard VXE, such as those built on top of Unicorn [46], e.g., [36, 48], by how they are specified: synthesized environments are specified using a declarative approach, rather than purely programmatically.

3 SYSTEM OVERVIEW

In this section we provide an overview of METAEMU, its inputs, and the assumptions we make about the firmware it can rehost.

3.1 Framework Architecture

We summarize METAEMU’s architecture in Figure 1. METAEMU takes as input one or more binary blob firmware and outputs a combined simulation/analysis environment capable of rehosting all the input firmware within a single VXE. In the combined VXE, each firmware has its own simulator (pink box in Figure 1). To synthesize these simulators, METAEMU requires four inputs: ❶ a processor specification, ❷ an execution mode specification, ❸ a list of execution observers, and ❹ a peripheral specification. To dynamically introspect and manipulate the firmware’s state, METAEMU attaches user-defined *observers* to the simulator, which can be triggered on, e.g., register reads and memory writes. The attached observers enable us to handle complex addressing modes (e.g., that used for the C166 architecture in §5.2.2) and implement symbolic solvers for peripheral checks (similar to *μEmu* [60] and Laelaps [5]). By interfacing with the analysis coordinator (gray box), observers can communicate with other rehosted devices (e.g., allowing one device to provide input to another’s peripherals) and share analysis facts, enabling inter-device analyses.

Framework Inputs. METAEMU is capable of rehosting many different types of devices; from those with bare-metal firmware to those

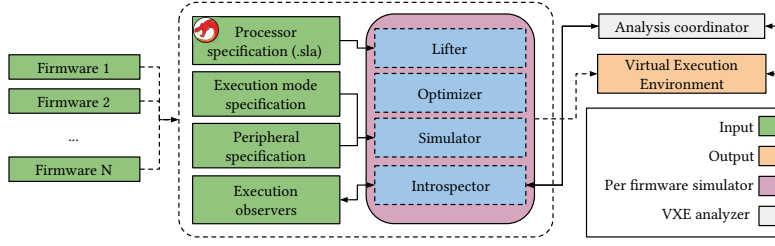


Figure 1: Overview of METAEMU. Each firmware along with corresponding processor, execution mode, and peripheral specifications are used to synthesize a simulator. Each simulator (pink box) can have execution observers attached, which monitor and manipulate its execution state and interface with an analysis coordinator (gray box) to facilitate inter-firmware interaction and analyses. The resulting VXE (yellow box) is composed of many per firmware simulators operating in parallel.

based on embedded RTOSes, such as ThreadX. Regardless of the type of firmware being rehosted, we make the following assumptions:

- (1) We do not have access to the firmware’s source-code.
- (2) We know its basic memory map and architecture.
- (3) We know the memory regions it uses for memory-mapped I/O with its peripherals.
- (4) We have a Ghidra language definition for its architecture.

Our assumptions are consistent with existing approaches, such as P²IM [18, 19] and μ Emu [60, 62], which also require manual specification of the memory mappings for each target firmware/device.

In addition to the firmware to rehost, METAEMU requires four auxiliary inputs to synthesize a VXE (shown in green in Figure 1).

Processor specification: To disassemble and obtain an architecture independent representation of each firmware, METAEMU leverages Ghidra’s language definitions. These consist of a *pspec* which defines register name and basic memory mappings, a *cspec* which defines calling conventions and size information of primitive types, and a *slaspec* which describes how to disassemble the architecture’s instructions and an encoding of their semantics. At the time of writing, there are 28 processor families supported in Ghidra master branch and many others created by the community.

Execution mode specification: METAEMU can simulate each firmware’s execution using different strategies (further detailed in §4.2.1), including concrete execution and concolic execution. Each specification defines how METAEMU simulates firmware at the level of individual Intermediate Language (IL) operations and how we represent the firmware’s state. All mode specifications implement a common interface and each synthesized firmware simulator is parameterized by a generic type constrained by that interface, allowing it to be instantiated to operate under any execution mode.

Execution observers: To extend each synthesized simulator to support architectural nuances, peripherals, interrupts, and user-defined analyses, we use so-called observers. As discussed later in §4.3, our observers intercept events during simulation specific to the simulator’s execution mode, and in response, can modify the firmware’s state and coordinate with other simulators and observers through a VXE-shared *analysis coordinator*.

Peripheral specification: As detailed later in §4.4, METAEMU supports peripherals through generic and user-specified models (§4.4.2), and automatic model inference (§4.4.1). We specify all types

of peripheral using execution observers, which we attach to simulators via their introspection interface. This interface is flexible and can support peripherals that receive input from outside of a VXE, enabling us to interact with rehosted firmware via SocketCAN, fuzzers such as AFL [59], and even physical devices.

3.2 Challenges Rehosting Complex Firmware

Fundamentally METAEMU is a multi-target emulation framework purpose-built to facilitate complex security analysis that can be customized and extended using a specification-based approach to alter execution policies, architecture definitions, and peripheral models. We encountered several challenges during the design and implementation of METAEMU. In this section, we provide an overview of these difficulties and how we have addressed them.

Architecture support and IR optimization: To facilitate architecture agnostic analysis, METAEMU emulates a firmware by first translating its architecture-specific instructions to an intermediate representation, and performs emulation of the resulting Intermediate Representation (IR) operations. The emitted operations are based on Ghidra’s SLEIGH language definitions for the target’s architecture. These definitions produce an IR representation that is not well suited for emulation, as it is overly verbose, as shown in Figure 2a. This is particularly problematic when using a symbolic execution policy, as a more complex IR leads to more complex symbolic formula. To improve the performance, we implement an IR optimizer in our lifter, which can produce a much more optimal IR representation, as shown in Figure 2b.

While our lifting and optimization approach is mostly standard, i.e., optimizations are applied on the SSA form representation of our IR, due to our use of SLEIGH specifications to generate our IR, we encountered a number of additional challenges in our implementation. The first being that Ghidra’s language definitions allow for variables (both registers and temporaries) to overlap. SLEIGH represents each variable as a (*offset, size*) pair that indexes into a flat address space, e.g., the register RAX might have offset 0 and size 8, while EAX might have offset 4 and size 4. This complicates SSA transformation, as it assumes that variables do not overlap. We thus, modify the standard algorithm to treat overlapping variables as equivalent. A further challenge is that SLEIGH’s temporaries have a liveness that only spans a single instruction’s IL operations. Hence, the same temporaries may be reused between consecutive instructions. We adapt the standard liveness data-flow analysis to

account for this implicit lifetime information by providing unique labels for temporaries across instructions, thus preventing data-flow information propagating over instruction boundaries.

Missing analysis state and context: When emulating embedded firmware, we often have to deal with missing or inconsistent state. For example, the values of a device’s peripheral status registers, or global variables that may have been set to particular values when the firmware was dumped, which prevent the firmware executing correctly when starting emulation from another location. Under these circumstances, the emulated firmware will usually stall in a check-and-wait loop. To solve this problem automatically, we implement a peripheral check solver, which ❶ identifies *looping* states and ❷ updates the firmware’s context with suitable values to allow execution to proceed. The main difficulty is how to detect such states during emulation. A naive approach would be to track and count the number of times blocks of operations are executed and if a particular block is executed repeatedly over a threshold number of times, we assume that the emulated firmware has entered a stall-state. While such an approach works, in practice, it is both inefficient and requires a significant amount of resources. To efficiently address this in METAEMU, we use a state machine-based approach, shown in Figure 3 to detect stall-states based on both code and memory access patterns, which reduces the amount of program state to track simultaneously.

While our peripheral solver can be used to bypass checks that do not impact the behavior of the target firmware with respect to a particular analysis, when the data or functionality of the peripheral does matter for a given analysis, we cannot simply bypass a stall-state check with *any* satisfying state configuration. Examples of this include the CAN peripheral of our RH850-based firmware (§5.2.4) and the Compare and Match Timer of our C166-based firmware (§5.2.2). In such scenarios, the peripheral’s behavior needs to be explicitly modeled. As even SoCs from the same family have slightly different implementations of such peripherals, and different kinds of context switching logic, it is both error-prone and time-consuming to implement versions of the same peripheral for different devices. To address this issue, we provide a universal peripheral backend (§4.4.2) and interrupt model. They abstract the peripheral behaviors and provide building blocks for implementing peripherals for different devices. Our interrupt framework enables a means to rapidly implement interrupt status tracking, context switching, and interrupt handler hooks and overrides.

Inter-device analysis: As mentioned in §2, a micro-controller may rely on the data from other chips or devices to function correctly. Modeling and analyzing the interactions between multiple targets pose two sets of challenges. Firstly, devices being rehosted in the same VXE may come from different manufactures, have different methods of handling peripherals, and may be based on different architectures. Secondly, the devices may lack a documented shared channel for communication, that would otherwise be facilitated by *black-box* hardware in a real-world setting. In METAEMU, we overcome the first set of challenges by providing a wide-range of architecture support and three methods to implement peripheral models. We address the second challenge by providing an analysis coordinator that facilitates message passing using a common interface between both device’s emulated peripherals.

4 IMPLEMENTATION OF METAEMU

In this section, we describe METAEMU’s key features in depth and detail how they can be used to analyze rehosted firmware. METAEMU is written entirely in Rust and spans ~40kloc (excluding comments and dependencies). This includes ~24kloc for *IR lifting and optimization*, ~5kloc for *IR simulation and observers*, and ~11.5kloc for *symbolic execution and other execution policy backends*. We do not rely on Ghidra’s code-base for any functionality, other than its XML-based processor specifications.

4.1 Lifting & IR Generation

To support emulation in an architecture agnostic way, METAEMU operates on an IR that explicitly models all processor instructions and their side effects. We represent each architectural instruction as one or more IL operations, which we obtain by a process called lifting, i.e., the translation of bytes into IL operations. Our IR is inspired by Ghidra’s [43] IR, P-Code [42]. In contrast to P-Code, our IR uses two isomorphic IL encodings: a SSA-form expression-based variant, which we use for optimization, and a Register Transfer Language (RTL) variant, semantically equivalent to P-Code, which we use for emulation. Similar to P-Code, our IR supports arbitrary extensions via intrinsic operations, which we use to model dynamic processor state changes, such as localized address mode switches.

Our lifter takes as input unmodified Ghidra language definitions, which contain information about calling conventions and the necessary information to lift a byte stream into our IRs. This approach enables us to make use of the vast number of processor architecture definitions from Ghidra and greatly reduces the workload of adding support for new architectures to METAEMU. Inspired by B2R2 [30], our lifter is completely parallel, and supports lifting chunks of the same firmware across many cores.

While one might assume we could have used Ghidra’s lifter as a basis for METAEMU, unfortunately, it does not perform any optimization of the IR it generates—it simply produces a literal translation of the specification for each instruction into IL operations—which we find leads to as much as 25% of the operations emitted being superfluous (§5.1.4). Clearly, naively interpreting IL operations emitted from Ghidra’s lifter will be inefficient, and for analyses such as symbolic execution will lead to much more complex formula due to extraneous operations. Figure 2a provides a taste of just how inefficient the generated IR is.

IR Optimization. In METAEMU, we address these inefficiencies in two ways. First, within our lifter, we rewrite and optimize our IR prior to it being emitted and processed by our simulator. Second, we cache optimized IR blocks, both on disk and within a cache shared among all executor instances of the same firmware, which enables us to amortize the overhead of performing our optimizations. Accordingly, METAEMU lifter can produce a much more optimal IR representation, as shown in Figure 2b.

We optimize IR blocks by rewriting and simplification using e-graphs [50]. This enables us to obtain the most optimal representation of each statement with respect to our rewrite rules. For e-graph construction and manipulation, we use egg [57].

We use our SSA-form expression-based IR, to perform our optimizations, rather than our RTL-based IR, to ensure the correct application of our rewrite rules in the presence of instruction-local

```

1 // mov dword [RBP - 0xc], ECX
2 var0620 := RBP + 0xffffffffffffff4
3 var1790 := ECX // redundant variable var1790
4 *var0620 := var1790
5 CF := 0x0
6 OF := 0x0
7 // xor ECX, ECX
8 ECX := ECX ^ ECX // ECX is constant value 0x0
9 RCX := zext(ECX, 64) // Zext of 0 is constant 0x0
10 SF := ECX < 0x0 // Constant 0x0
11 ZF := ECX == 0x0 // Constant 0x1
12 var2580 := ECX & 0xff // Constant 0x0
13 var2590 := popcount(var2580) //number of 1s in 0 is 0
14 var25a0 := var2590 & 0x1 // Constant 0x0
15 PF := var25a0 == 0x0 // Constant 0x1

```

(a) IR produced by Ghidra’s lifter. The highlighted lines indicate instructions that can be simplified.

```

1 var0620 := RBP + 0xffffffffffffff4
2 *var0620 := ECX
3 CF := 0x0
4 OF := 0x0
5 ECX := 0x0
6 RCX := 0x0
7 SF := 0x0
8 ZF := 0x1
9 PF := 0x1

```

(b) Optimized IR produced by METAEMU for the sequence in Figure 2a. The optimization to “mov dword [RBP - 0xc], ECX” eliminates the intermediate variable var1790. The optimization to “xor ECX, ECX” uses an identity for XOR, i.e., $v \oplus v = 0$. Our optimizations are *safe* and preserve both memory and register side-effects.

Figure 2: Generated IR for the x86-64 instructions: mov dword [RBP - 0xc], ECX; xor ECX, ECX.

control-flow. Such control-flow occurs when the IR corresponding to an architectural instruction requires loops or branches to model the architectural semantics fully (e.g., rep stosb). Thus, an IR block is more akin to a sequence of instruction-level control-flow graphs, rather than a strict basic block.

After obtaining the SSA-form representation, we transform each statement into an e-graph, merge it into a block-level e-graph, and apply rewrite rules which cover algebraic identities and simplifications. Upon adding a new statement to the block-level e-graph, we greedily apply rewrite rules, and extract its most optimal representation with respect to AST depth (i.e., the shallower, the better). By extracting statements in this way, we preserve the original IR ordering, and by constructing an e-graph for the entire block incrementally, we preserve the equivalence classes discovered, allowing each statement to benefit from any rewriting possibilities applied to its predecessors. Finally, we use liveness analysis [1] to identify redundant assignments and remove them.

Our optimizations preserve all side-effects to memory and registers encoded in our unoptimized IR and therefore will not negatively impact the accuracy of any downstream analyses performed. To the best of our knowledge, our use of e-graphs for optimizing IR for emulation is novel. In evaluating our approach (§5.1), we find that through IR optimization and designing our emulator specifically for rehosting, we achieve more than 400% performance improvement over Ghidra’s lifter and emulator.

4.2 Firmware Simulation

At the most fundamental level, the simulator METAEMU generates load an input firmware, translate its instructions into our IR, and interpret each emitted IL operation. Within the output VXE, each simulator runs in parallel on a separate thread, and communicates using a shared analysis coordinator.

4.2.1 Execution Modes & Policies. The method each simulator uses for interpretation depends on the execution mode or policy it was synthesized with. In contrast to traditional emulation environments, METAEMU supports a variety of execution modes to simulate the execution of a rehosted firmware. Among other scenarios, these modes allow us to address the lack of complete peripheral models

and support analyses bootstrapped using incomplete execution contexts, which often occur when analyzing firmware extracted from end-user devices. Each policy also influences the kind of observations that attached execution observers (§4.3) can make and the underlying representation they act upon. We support five modes:

❶ **Concrete execution** follows the standard semantics of the firmware’s Instruction Set Architecture (ISA). It represents state as a collection of byte arrays, and updates the state by directly interpreting each IL operation in a step-wise manner.

❷ **Concolic execution** [49] permits us to mark some input variables, i.e., memory locations, as symbolic, while treating the remainder as in concrete execution. We obtain concrete assignments for symbolic variables by querying the Satisfiability Modulo Theories (SMT) solver, Boolector [44]. By negating the path constraints associated with a branch, we can obtain an assignment that allows us to explore both branch targets. Under this policy observers can inject symbolic values into the firmware’s state.

❸ **Forced execution** [45] follows concrete execution semantics, with the caveat that at conditional branches, we can “flip” the branch condition, such that the non-satisfying branch target is taken.

❹ **Micro execution** [22] follows concrete execution, with the exception our observers can intercept invalid memory accesses, map the locations into our VXE state, and populate them by an analysis-dependent policy.

❺ **Flood execution** [56] follows forced execution, with the additional property that all branch targets, regardless of their satisfiability, are explored in accordance with an exploration policy, e.g., to a fixed bound or threshold branch coverage. In METAEMU we implement a variant of flood execution based on micro execution, as proposed by Gotovchits et al. [23]. Under this policy, observers witness events from multiple execution paths simultaneously.

4.2.2 Architectural Nuances. To facilitate non-standard addressing, dynamic processor mode switches, and other architectural quirks, we provide an interface to implement IL intrinsic operations. This interface enables METAEMU to support functionality that cannot be directly modelled in our IR, e.g., instructions for cryptographic primitives, as well as modify how low-level operations such as

memory reads and writes are performed. We use this interface to support the *DPP override mechanism* address scheme for the C166 architecture [28], which requires us to alter how the simulator resolves memory accesses for a variable window of instructions.

4.3 Observers & Analysis Coordination

To extend our specification approach to support peripherals (§4.4), arbitrary extensions to our generated simulators (§4.5), and different kinds of analyses (§5.2), we use a concept called *execution observers*. Observers *attach* to our simulators and register to receive event notifications via each simulator’s *introspector* (bottom blue box in Figure 1). In response to events, we can configure observers to manipulate the running firmware’s state and/or interface with the VXE *analysis coordinator* (gray box in Figure 1) to enable inter-device communication or analyses.

As noted in §4.2.1, the kind of events an execution observer can witness, and the firmware state representation it operates on, is tied to the *execution policy* of the simulator it is attached to. However, regardless of the execution policy a simulator is synthesized with, we can register observers to receive event notifications for a number of basic event kinds. These include: **register reads/writes**, **memory reads/writes**, **program counter changes**, **conditional branches**, and **function calls**. We associate each event kind with a corresponding response kind, which we use to facilitate common rehosting tasks, such as: instruction skipping, conditional branch flipping, function call replacement, and forking the simulator’s state. We provide a full list of event kinds in Appendix A.

Inter-device analysis. Our analysis coordinator provides a generic message passing interface that routes arbitrary event notifications between each simulator. It also acts as an inter-device communication channel, that allows each rehosted device to communicate with any other device inside the same VXE. For example, it enables us to connect devices by their Hardware Abstraction Layer (HAL) APIs, without resorting to manually implementing low-level cross-device communication channels using emulated peripherals.

4.4 Peripheral Support

As discussed in §2, correct and faithful firmware simulation depends on providing some degree of peripheral support. When rehosting, this support is still required: for example, to supply input to the firmware when fuzzing, or to ensure the firmware can execute at all if it is based on a RTOS.

In embedded firmware, peripheral interactions are frequently performed using Memory-mapped I/O (MMIO). To facilitate this, such firmware has a continuous memory region allocated specifically for MMIO, which is divided into smaller regions for each peripheral. These regions contain memory mapped versions of a peripheral’s control and status registers, as well as registers facilitating data transfers between the firmware and peripheral. This presents two challenges when rehosting firmware: ❶ When executing, firmware frequently checks its peripherals’ statuses. If the status of a peripheral does not match what the firmware expects, e.g., due to being uninitialized, execution will “stall” in an infinite loop until the peripheral’s status changes. Thus, without correct support, execution cannot proceed past such checks. ❷ A firmware’s control-flow is often dependent on data read from its

peripherals. For example, for ECUs that communicate using Unified Diagnostic Services (UDS), the specific service handler executed will be determined by data received via a CAN peripheral. Hence, without peripheral support, it is impossible to faithfully explore such execution paths.

To overcome these obstacles, we provide three types of peripheral support in METAEMU, as shown in Appendix B. They are all based on execution observers (§4.3). The first, inspired by Lae-laps [5], is a **generic Peripheral Check Solver** that allows us to specify a MMIO address range and automatically bypass simple checking loops that would otherwise cause execution to stall. The second, is a **Universal Peripheral framework**, which provides a specification-based approach to build common peripherals by composing generic models. These models are *architecture-agnostic*, so can be reused for many different devices, with minimal reconfiguration. METAEMU provides models to act as generic input sources, e.g., for fuzzing or to facilitate inter-firmware communication, timers of various kinds, and models that allow a peripheral to be associated with one or more interrupts (discussed in §4.5). Finally, as some peripherals cannot be implemented using automated or generic approaches, but are essential to enable security analyses, e.g., complex I/O devices for communication over CAN, we provide an observers-based API (§4.3) to **manually implement peripherals**. We demonstrate this in §5.2.4 by implementing CAN network interface controller.

4.4.1 Inferring Expected Peripheral Behavior. Our peripheral check solver can be applied in many rehosting scenarios, as firmware often only performs comparisons against a peripheral’s status register to ensure it is initialized. These checks usually occur as tight loops whose exit condition depends on certain bits of a MMIO register being set or clear, similar to Listing 1. They generalize to the following: ❶ the firmware reads the peripheral’s MMIO register, ❷ it checks the value read using a boolean predicate, ❸ if the predicate yields false, the loop repeats, otherwise execution continues past the check. We use this pattern to identify peripheral checking loops.

```
do {
    mmioValue = read_4(0xffff81104);
} while ((mmioValue & 4) == 0);
```

Listing 1: Example of a peripheral checking loop.

Bypassing status checks: To compute *satisfying* values to exit checking loops, we use localized symbolic execution, as shown in Figure 3. Our technique works by monitoring and symbolizing read accesses to our configured peripheral MMIO region. For each access, we track its data-flow and build an expression tree capturing the constraints imposed upon the read value. Upon reaching a conditional branch that is dependent on our read value, we use a SMT solver [44] to find an assignment that enables us to explore the “not taken” branch target. We then execute the branch; if it leads us to re-enter of the checking loop, we replace the value read from the MMIO register with the value computed using the solver.

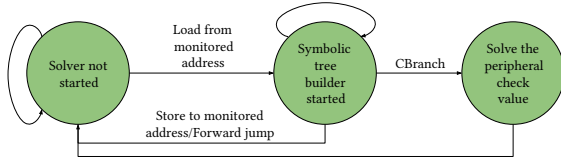


Figure 3: Peripheral model inference to bypass status checks. Our solver monitors loads from MMIO register addresses and builds an expression tree of the constraints imposed upon the value read. Upon reaching a conditional (cbranch), it uses SMT solver to compute an assignment for the register that allows us to exit the checking loop.

4.4.2 Universal Peripheral Models. Building support for common peripherals for many different devices is both tedious and error-prone. Thus, it is desirable to build generic peripheral models instead. However, different Microcontroller Units (MCUs) use different MMIO registers and bit masks to perform similar tasks, complicating the implementation process. For example, to control the start/stop of a CMT, the C167CR MCUs use bit 6 at address `0xff42` [28], while SH-2A MCUs use bit 0 at address `0xffec000` [47]. Our *universal* peripheral models overcome this difficulty generically.

Within METAEMU, we support *universal* peripherals using two methods. ❶ We provide an interface to intercept and redirect any function call, e.g., HAL API calls. This enables METAEMU to handle many kinds of I/O-based peripherals using generic handlers, without concern for the low-level hardware details. ❷ We provide memory/register read/write hooking, which enables us to model MMIO-based peripherals generically. Our MMIO peripheral models implement data and status handling logic using a common interface that enables them to be used with our universal peripheral framework. Our framework then allows us to configure each model declaratively by specifying the address, bit masks, and handler functions associated with a given peripheral’s MMIO registers. To facilitate model composition and architectural quirks, we provide a means to override each model’s handler functions, which enables us to modify and combine their behaviors arbitrarily. Listing 2 demonstrates how the CMSTR register of SH2A CMT can be configured using our generic CompareMatchTimer model.

```
let mut cmt = CompareMatchTimer::default();
cmt.map_function_addr_read(ADDR_CMSTR, 0x01,
                          &CMTFun::is_enabled);
cmt.map_function_addr_write(ADDR_CMSTR, 0x01,
                           &CMTFun::set_enable);
```

Listing 2: Configuration of a Compare & Match Timer model using our universal peripheral backend.

4.5 Interrupt Support

While many peripheral interactions occur synchronously, i.e., exclusively via MMIO, others happen asynchronously. A common example is the *tick* of a timer peripheral used in RTOS-based firmware to implement task scheduling. Such asynchronous events manifest in firmware via interrupts, which are handled by inducing a context switch to a so-called Interrupt Service Routine (ISR). This type of context switch is almost always facilitated by hardware, and works

by first saving a snapshot of the current execution context to a vendor-defined area of memory, and then redirecting control-flow to the interrupt handler routine. To return from an ISR, either the interrupt routine or the micro-controller itself will be responsible for restoring the execution context depending on the implementation of the vendor. These type of interrupts are commonly used in event driven firmware, where most functionality is implemented via ISRs. To handle this diversity in METAEMU, we provide a generic interrupt handling framework, implemented using observers.

Similar to our universal peripheral backend (§4.4.2), our interrupt handling backend is also specification-based. It enables us to specify an interrupt by configuring handlers for its triggering behavior and restoration logic. Within METAEMU, we provide a number of *default* interrupt behaviors, e.g., to associate an interrupt trigger with a peripheral, and to perform context restoration based on specified registers or memory ranges. Our backend tracks each configured interrupt’s *enabled* and *triggered* status, the ISR or analysis-specific functionality to perform when it is triggered, and the context restoration logic to execute after it has been handled. We provide a complete example in §5.2.5.

5 EVALUATION

We evaluate METAEMU using three criteria: ❶ performance, ❷ implementation flexibility, and ❸ real-world usability. For ❶ we benchmark METAEMU’s raw execution performance, and compare it to two existing tools for firmware emulation: Unicorn and Ghidra’s emulator. For ❶ and ❸, we measure the extent our lifter is able to optimize its generated IR for large ECU firmware images, and compare the number of emitted IL operations to naive lifting without any optimization. We assess ❷ and ❸ together through six case-studies, which demonstrate using METAEMU to perform different kinds of firmware analysis, including: inter-device analysis of two rehosted ARM firmware, inference of undocumented memory mapped peripheral interactions in a Renault BCM, reverse engineering of the UDS handler functions of a Land Rover Discovery’s TCU, fuzz testing to rediscover a backdoor in the “Security Access” UDS service of a Volkswagen Passat’s IC [14], and emulation of the ThreadX RTOS implementation of a Range Rover Evoque TCU. Across our case studies we demonstrate that METAEMU is capable of enabling complex dynamic analyses built upon symbolic execution, fuzz testing, and micro execution [22].

We perform our experiments on a machine with a 32-core AMD Ryzen Threadripper 3970X and 128GB RAM.

5.1 Performance Benchmarks

We evaluate the performance of METAEMU using two metrics: execution time and optimization of emitted IL operations. In the evaluation of execution time, we compare our tool with two existing emulation frameworks: Unicorn and Ghidra. We compare METAEMU to Unicorn, as it is widely used for rehosting and performing security analyses [35, 36, 48], and to Ghidra’s emulator, as it is used as the backend for `af1_ghidra_emu`, a fuzzer released by Airbus targeting esoteric architectures [2]. We use ARM programs for our head-to-head benchmarks based on the assumption that it is the most optimized embedded architecture all tools support.

We perform four sets of experiments: ❶ a micro-benchmark to evaluate the performance of each tool on various analysis tasks, ❷ a deeper inspection of the differences in performance between Unicorn and METAEMU performing different kinds of hooking, ❸ an evaluation of the performance and trade-offs of performing IR optimization, and ❹ the effects of IR optimization on the number of IL instructions emitted.

5.1.1 Micro-benchmarks. We benchmark the performance of each tool on the programs described in Appendix C and visualize the results in Appendix D. Our test harnesses measure execution time in milliseconds; we run each test 10,000 times and report the average time taken. We omit the results for Ghidra’s emulator, as they are significantly worse than both tools shown—on average by at least an order of magnitude, e.g., “1M-no-count” takes 3234ms, compared to 271ms for METAEMU and 385ms for Unicorn.

We find that METAEMU performs favorably compared Unicorn on all but one benchmark. We attribute the performance difference between METAEMU and Unicorn on the “loop3-2loop” benchmark, to be due to the program being well suited to optimization by Unicorn’s JIT compiler, as it contains a small number of basic blocks executed in two tight loops, where both loop bounds are hard-coded.

5.1.2 Deeper Analysis of METAEMU and Unicorn. In this experiment, we benchmark the performance of METAEMU and Unicorn while analyzing a sample program that consists of 100k instructions performing repeated memory transfer operations and function calls. In addition to baseline performance, we benchmark three different kinds of analyses: execution trace logging (PC Change Hook), memory access interception (Memory Hook), and function stubbing and call context logging (Call Hook). We include two baselines for METAEMU—one with IR optimization and one without. We run each experiment 10,000 times and report the average time taken. We do not include Ghidra’s emulator in these experiments, as it does not provide sufficient hooking support and is dramatically slower than both METAEMU and Unicorn.

Results: We show the results of our benchmarks in Appendix E. Across all benchmarks, Unicorn is on average ~ 20 times slower than METAEMU. For Memory Hook and PC Change Hook, both METAEMU and Unicorn have negligible performance overhead over baseline performance, while for Call Hook, both tools show larger overheads, which is due to the additional complexity of logging calling contexts. METAEMU’s IR optimizations provide an average of 4-5% performance improvement. Our benchmarks clearly demonstrate that our specification-based rehosting approach can perform at least as well as those based on Unicorn—without a performance trade-off—while also being much easier and flexible to extend.

5.1.3 IR Optimization Performance and Trade-Offs. In this experiment, we analyze the trade-offs of IR optimization by performing an extended analysis of the the “loop3-2loop” program from §5.1.1 compiled for both ARM and C166 (omitted for Unicorn as it does not support C166). We measure the time each framework takes to execute the program’s loop 1k times and 65k times, and measure the overheads of performing METAEMU’s IR optimizations both online and offline against a baseline without any optimizations enabled.

Results: Appendix F shows the benchmark results. METAEMU’s optimization overhead is constant for both architectures on both

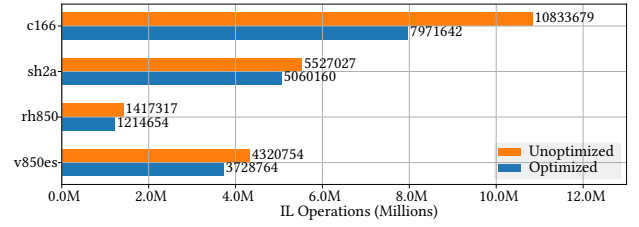


Figure 4: IR optimization performance for each ECU firmware. Total number of operations calculated by lifting every basic block of each firmware; reduction calculated by number of eliminated operations.

test configurations— ~ 15 ms for C166 and ~ 2 ms for ARM. As mentioned in §5.1.1, Unicorn outperforms all frameworks on this benchmark, due to its JIT optimizer. We find that although METAEMU and Ghidra’s emulator share the same processor specifications, METAEMU is $\sim 400\%$ faster on all benchmarks for both architectures. METAEMU performs most favorably when applying its optimizations offline, and when applying its optimizations *online*, we only observe favorable performance on the longer running loop. On the shorter loop, the overheads induced by optimization (C166: ~ 15 ms, ARM: ~ 2 ms) result in diminished performance. Thus, we find that the choice of whether to apply optimizations depends on the kind of analysis being performed and the size of the program being analyzed. We provide an option to disable optimizations as part of our synthesizer specification. As a rule of thumb, optimizations make most sense when running loop-based firmware, fuzzing, or when performing symbolic execution (due to the decreased size of symbolic formulas), and otherwise may negatively impact performance.

5.1.4 Impact of Optimizations on Real Firmware. To evaluate the effectiveness of our optimizer on real-world firmware, we measure the total number of IL operations before and after optimization when lifting every basic block in each of our ECU firmware. The C166-based IC firmware is ~ 512 KB and contains 2609 functions, the RH850-based TCU is ~ 32 KB and contains 646 functions, the V850ES-based BCM is 544KB and contains 2987 functions, the SH-2A-based TCU is 8.4MB and contains 14,223 functions.

Results: We summarize METAEMU’s optimizer performance by IL elimination in Figure 4. Though our results are a conservative approximation of our tool’s performance—accounting only for optimizations that lead to elimination of IL operations—across all firmware we see reductions of hundreds of thousands of operations, e.g., for our C166-based firmware, we observe that METAEMU reduces the number of operations by $\sim 27\%$: from ~ 10.8 M to ~ 7.9 M.

As our optimizations can be applied offline, they incur no overhead during simulation. However, when lifting, applying IR optimization induces a non-negligible overhead of $\sim 700\mu$ s per IR block, compared to $\sim 6\mu$ s without. The optimization time is constant regardless of the number of iterations. We attribute the significant difference to our use of e-graphs and equality saturation [57] to find optimal IL sequences—our optimizer effectively computes all simplifications of each IR block and extracts the most optimal with respect to minimizing the IR size.

Table 1: Summary of case studies performed. METAEMU features evaluated: architecture support (A), inter/multi-device analysis (M), peripheral support (P), interrupt support (I), integration with external tools (T). Implementation size shows the approximate LoC for experiment (E) and specification for peripherals and execution mode (S).

Firmware	ISA	Impl. Size		Firmware Evaluated					
		E	S	A	M	P	I	T	
Arduino & NuttX firmware	ARM	300	180	✓	✓	✓	-	✓	
P ² IM firmware (averaged)	ARM	200	170	✓	-	✓	-	✓	
Volkswagen IC	C166	260	100	✓	-	✓	-	✓	
Renault BCM	V850E2	160	<10	✓	-	✓	-	✓	
Land Rover Discovery TCU	RH850	700 ^δ	-	✓	✓ [‡]	✓	-	✓	
Range Rover Evoque TCU	SH-2A	370	110	✓	-	✓	✓	✓	

δ: We manually implemented complex peripheral (CAN Bus) with hooking API
[‡]: We rehost multiple instances of the firmware to perform fuzzing.

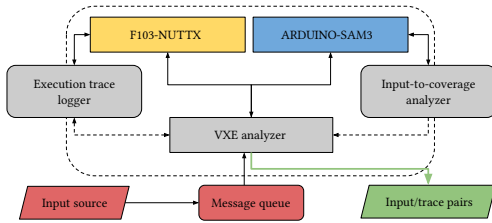


Figure 5: Inter-device analysis. Inputs are supplied outside the VXE via a message queue, received by the F103, and forwarded to the ARDUINO. The F103 has an observer that logs the execution path corresponding to each input received and sent. The ARDUINO has an observer that analyzes the branch coverage corresponding to processing received inputs; on new coverage, it notifies the shared VXE analyzer, which instructs the F103’s observer to dump the execution trace matching the last sent input. The VXE analyzer outputs input/trace pairs that yield new coverage.

5.2 Case Studies

In this section, we show how METAEMU can be used to emulate and analyze firmware based on five different ISAs: ARM, C166, RH850, SH-2A, and V850E2—the latter four are not supported by any existing rehosting framework. We show that METAEMU handles complex end-user firmware by rehosting four ECU firmware. We also perform two other case studies: inter-device analysis (§5.2.1), and fuzzing and rehosting non-automotive firmware (§5.2.6), using ARM-based firmware from the P²IM data-set [19]. The firmware from this data-set are simpler than our ECU examples, and are chosen to enable us to more easily describe our experimental set-up and results. We summarize our case studies in Table 1.

5.2.1 Inter-Device Analysis. In this case study, we demonstrate METAEMU’s capability to rehost multiple firmware in the same VXE and perform an inter-device analysis. Each target firmware is ARM-based and adapted from the P²IM [19] data-set—one is based on the Arduino SDK, and the other on NuttX, as shown in Figure 5.

Objective: The goal of this case study is two-fold: First, to show how two rehosted firmware can communicate, where one firmware

(F103) is supplied input from outside the synthesized VXE, and the other (ARDUINO) receives input from the other rehosted firmware (F103). Second, to demonstrate an analysis that captures execution traces from a rehosted firmware (F103) that leads to new branch coverage in another (ARDUINO). This case study models a typical scenario found in CAN networks, where one can only interact with a particular ECU by sending messages via another.

Set-up: We develop five observers. Three simulate peripherals: one to receive input via UART (outside to F103), one to transmit data via a TTY (from F103) and one to receive input via a serial port (into ARDUINO). Two perform analyses: an execution trace dumper that starts on a *read* from UART and stops on a *write* to a TTY, and a coverage tracker, which reports new branch coverage via the VXE’s coordinator. The coordinator is configured to dump execution trace/input pairs that cause new branch coverage. We provide input to the F103 using random byte sequences, and specify a *concrete execution mode* for each firmware.

Discussion & results: Combined, our firmware configuration spans ~180 lines of code (not including processor specifications), while our observers take a further ~300. Our configuration accounts for overriding firmware functionality unrelated to our analysis task, creating a memory mapping for each firmware, and specifying the behavior of our analysis coordinator. Each rehosted firmware executes in parallel and faithfully simulates its expected behavior. This case study demonstrates how our approach can enable an otherwise tricky to reproduce analysis scenario with very little manual overhead. Further, it shows how METAEMU can facilitate modeling peripheral and inter-device interactions, akin to those that regularly occur in real automotive networks, without requiring any hardware or source-code access.

5.2.2 Volkswagen Passat Instrument Cluster (C166). In this case study, we demonstrate how METAEMU can be used with LibAFL to rediscover a previously reported backdoor in the UDS “Security Access” service of a Volkswagen Instrument Cluster [14]. The ECU is based on the Infineon C166 architecture. To support the C166 architecture, which is not currently distributed with Ghidra, we base our language definition on an open-source project [16]; our definition consists of 1737 lines. We implement two extensions to our simulator: an intrinsic to handle the C166’s *DPP override* addressing [28], which enables the firmware to override which memory pages are accessed for a variable window of instructions, and an observer to implement its GPR bank switching.

Objective & set-up: The backdoor is embedded in the UDS handling routine. The routine receives two inputs: a buffer containing the UDS request, which we populate with input from LibAFL, and a request ID, corresponding to a UDS service, which we populate using the ID of the “Security Access” service (0x27). Authenticating against this service enables a client to access security critical services, e.g., “Request Download” (ID 0x34), which permits new software to be transferred to the ECU. To authenticate, a client must complete a challenge-response handshake by sending a correct *key* for a given *seed*. The backdoor enables this check to be bypassed by supplying a specific hard-coded value in the request buffer (0xCAFFE012). The backdoor trigger is in the form of two 2-byte comparisons, and can easily be discovered by fuzzing. To

do so, we configure our LibAFL harness to mark inputs that reach blocks corresponding to successful authentication attempts as if they induce a “crash”.

Discussion & results: We were able to trigger the backdoor with our fuzzer, but not as easily as expected. In fact, our initial attempt was unsuccessful, as the firmware relies on a timer peripheral to correctly execute the “Security Access” check—instead of validating our fuzzer’s supplied “key”, it enters an infinite polling loop. On investigation, we found that this check first generates a challenge seed by repeatedly sampling from the timer’s value register until a specific criterion is met. Rather than bypassing the seed generation, we attached a peripheral to the firmware’s simulator based on our generic CMT model (§4.4.2). The specification takes just 6 lines; requiring masks for the enable bit, toggle on match bit, and current tick value, and the address range of the MMIO of the timer peripheral. Our peripheral model emulates realistic behavior in our simulator when accessing the timer’s memory mapped registers, TxCON and Tx, successfully enabling us to fuzz the firmware to discover the backdoor key.

5.2.3 Renault Body Control Module (V850E2). In this case study, we use METAEMU to aid in identifying peripheral access checks in firmware from a Renault BCM. Even when an emulator is available for the architecture of a device, one of the major obstacles when performing rehosting is the lack of documentation for its peripherals. Usually, processor manuals provide the address range of MMIO registers, but as each device can have a diverse array of peripherals, inferring the meaning of each address often requires manual reverse engineering. Unfortunately, when these documents are not in the public domain, we need to reverse engineer the MMIO range itself to achieve even basic emulation. In this case study, we show how METAEMU can help automate this task.

Objective & set-up: The objective of this case study is to facilitate basic emulation of our BCM firmware, and identify peripheral access checks, without prior knowledge of specific peripheral register addresses. We use processor definitions adapted from those distributed with Ghidra. We obtain an approximate MMIO peripheral address range from the processor manual of a related MCU (V850E2/Fx4-G), as the peripheral manual for the MCU (V850E2/Dx4) used in the BCM is not publicly available.

Identifying peripheral status checks: We perform our analysis in two steps. We first use our peripheral check solver to identify peripheral checking loops using registers mapped to the MMIO range of a similar MCU (0xffff40000–0xffff8000). This enables us to identify and bypass some peripheral checks, however, our firmware still *stalls* prior to reaching its main loop. To overcome this, we gradually widen our assumed MMIO range by specifying larger bounds in our solver’s configuration. After a few iterations, we determined that the real MMIO range of the MCU is much wider than expected: we discovered checks in the range 0xffff8000–0xffffffff. By reconfiguring our peripheral check solver to use this extended range, we were able to bypass the initialization checks performed by the firmware. This case study demonstrates that our specification-based approach can enable analyses of this kind without custom peripheral models, or device-specific heuristics.

5.2.4 Land Rover Discovery Telematics Unit (RH850). In this case study, we use METAEMU to rehost the TCU from a 2018 Land Rover Discovery in order to reverse-engineer its UDS handler routines. To aid our reverse-engineering, we use fuzzing to identify *valid* UDS requests. The ECU’s firmware is based on the RH850 architecture. It’s worth mentioning that despite the RH850 and V850 are from similar microcontroller family, there are still differences in instruction set and the peripheral layout.

Objective & set-up: TCUs are responsible for communicating with and monitoring other ECUs on the CAN bus, and reporting diagnostics data and metrics over other mediums, such as LTE, hence have a large attack surface. UDS is the protocol responsible for transmitting diagnostic information and is implemented on top of CAN. Among other functionality, UDS can be used to re-flash or dump an ECU’s firmware. The goal of our analysis is to reverse engineer the UDS handling functions in our target firmware. These functions take input from a CAN peripheral, process it, and act accordingly. To analyze them, we take a four-step approach:

- (1) Since UDS is a CAN-based protocol, to determine how to use it to communicate with the device, we first need to identify the device’s CAN IDs.
- (2) Next, to interface with the device’s rehosted firmware over UDS, we create a model for its CAN peripheral.
- (3) As the firmware interfaces with many peripherals unrelated to our analysis task, yet relies on them being successfully initialized to configure its internal state prior to executing its main loop, we attach a peripheral check solving observer to supply suitable values when accessing their MMIO registers.
- (4) Finally, to identify valid UDS requests, we use a LibAFL-based fuzzer to supply input to the firmware via its CAN peripheral, and track which inputs lead to new coverage.

CAN ID identification: In a modern automobile, the CAN bus is the standard medium for ECUs to communicate with each other and the outside world. Thus, it is usually the first interface/input source we investigate when analyzing automotive firmware. On the CAN bus, each ECU is assigned one or more CAN IDs, and will only respond to messages sent to those IDs. As many manufacturers attempt to keep CAN IDs secret, it is a non-trivial task to identify them effectively without analyzing the ECU’s firmware.

As mentioned previously, automotive microcontrollers usually interface with their peripherals and, thus, the CAN bus, by reading and writing to MMIO registers. Each such register controls either a peripheral’s behavior or act as an input/output buffer. From our experience, for peripherals that interface with the CAN bus, one register will contain the *listening* CAN ID. Hence, if we know the address this register is mapped to, we can use it to recover the IDs the ECU *listens* on by monitoring values written to it.

Unfortunately, exhaustively enumerating all execution paths that write to the register requires near complete emulation of the entire firmware—defeating the purpose of rehosting. Flood execution [56], however, provides a means to approximate all execution paths in a bounded manner, and the micro execution-based variant proposed by Gotovchits et al. [23] provides a means to perform flood execution in the presence of failing memory accesses. To recover CAN IDs, we use *flood execution* mode with our synthesized simulator to enumerate paths, and use an observer to log writes to the register

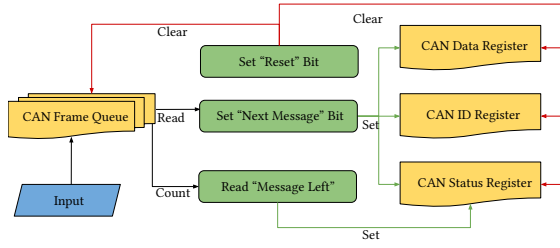


Figure 6: Data-flow diagram of RH850 CAN peripheral. We store incoming CAN messages in a FIFO queue (blue box). When the firmware sets the “next message” bit, we dequeue a CAN frame, use it to populate the CAN data and CAN ID registers, and then set the data available bit in the CAN status register. Upon a *reading message left* event, we update the “message left” counter in the CAN status registers with the length of the queue. When the firmware sets the peripheral’s “reset” bit, we clear the queue and reinitialize the registers.

documented to store CAN IDs. Through this process we recover three CAN IDs: 0x7df, 0x18db33f1, and 0x700.

CAN peripheral modeling: We model the device’s CAN peripheral using observers, as shown in Figure 6, and interact with our model via SocketCAN [55]. We use an observer to hook *reads* and *writes* to the CAN registers to simulate receiving and sending CAN frames. When sending data, we build CAN frames using values from the CAN status register (TMSTS), the receive ID register (RFID) and receive data register (RFDF); after transmission, we set the firmware’s transmission success bit. When receiving data, we read a frame from our input source, and use it to set the following registers: TMC, TMID, TMPTR, and TMDF.

Bypassing peripheral status checks: To bypass the initialization checks of the device’s other peripherals, we use our symbolic status check solver (§4.4.1). We configure it using the full peripheral address range: 0xFF400000–0xFFFFAFFF. Alongside our CAN peripheral, this enables us to execute the firmware from reset to its UDS request processing loop.

Fuzzing for valid UDS requests: To fuzz for valid UDS requests, we use *concrete execution* mode to run our rehosted firmware from reset to the UDS function, and then use an observer to take a snapshot of the simulator’s state. We build a LibAFL-based harness which starts execution from our snapshot and supplies input to the UDS routine via our CAN peripheral. We implement a custom EventManager for LibAFL that supports sharing coverage and *interesting* inputs across multiple METAEMU simulators via our *analysis coordinator*. This enables us to rehost many instances of our firmware and fuzz the UDS routine in parallel. Through our analysis, we generated inputs that explored execution paths covering 898 unique IL branches, which uncovered 8 UDS request handlers.

5.2.5 Range Rover Evoque Telematics Unit (SH-2A). In this case study, we demonstrate how METAEMU can be used to rehost a Range Rover Evoque TCU SuperH-2A firmware. The firmware is based on ThreadX RTOS, which executes multiple tasks concurrently. To rehost, it requires robust peripheral models to correctly perform task switching—something that cannot be achieved using simpler

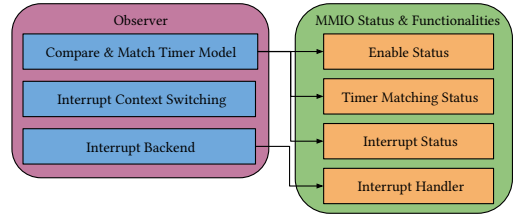


Figure 7: Overview of our SH-2A CMT model, which is responsible for tracking the enabled, timer matching, and interrupt status of the peripheral. We use our interrupt backend to specifying a custom interrupt handler and ensure the PC and SP registers are preserved during the context switch.

symbolic modeling approaches, such as the peripheral check solver used in our other case studies.

Objective & set-up: Through manual reverse engineering, we found that the firmware uses a timer interrupt to facilitate task scheduling, which is performed by a CMT peripheral. The goal of this case study is: First, to show how METAEMU facilitates implementing a complex peripheral that can faithfully trigger task switches. Second, to show how METAEMU can emulate hardware-supported multi-tasking.

Discussion & results: Since the device’s CMT peripheral acts as both a timer and interrupt source, we can implement it using a combination of our generic CMT model (§4.4.2) and our interrupt backend (§4.5), as shown in Figure 7. To configure our CMT model, we specify the mapping between the peripheral’s registers and the model’s set/unset actions. This enables our model to update and track its enabled status, interrupt status, and timer matching status. To simulate the timer’s counting and interrupt triggering behavior, we implement a simple observer that increments the timer’s value by one each time a new architectural instruction is lifted, and *fires* an interrupt using METAEMU’s interrupt backend. Our implementation (optimistically) assumes that each instruction takes one clock cycle, and the timer increases based on the device’s clock. We configure our interrupt backend to trigger a jump to the firmware’s timer ISR when it is instructed to *fire* by our timer observer. Since the context switch is normally performed in hardware, we configure METAEMU to preserve the status register SR and program counter PC prior to jumping. The firmware uses the *rte* instruction to return from interrupt handlers, and its logic is implemented in the architecture’s processor specification. Our peripheral requires just ~250 lines of specification and code. To test our peripheral model, we attach an execution tracer observer to our simulator and run the device from reset. Our traces show that the emulated firmware correctly performs task switches and mirrors the real firmware’s behavior.

5.2.6 P²IM dataset firmware. The P²IM authors [19] provide a dataset consisting of 10 ARM-based firmware based on open-source projects, which all use a HAL to interact with their peripherals. In this case study, we use the Gateway and Soldering_Iron firmware to demonstrate the correctness of METAEMU and show that it can achieve the same analysis outcomes as existing rehosting frameworks. We perform two experiments: ❶ we fuzz test the Gateway

firmware, and ② we use the Soldering_Iron firmware to test METAEMU’s support for handling tricky (DMA-based) peripherals. **Set-up:** For experiment ①, we set up a basic fuzz harness to supply I2C query packets by hooking the HAL of the firmware. Similar to past work [41], we mark part of the firmware’s memory as a “red zone” (write permission disabled) to perform sanitization and detect any memory corruption bugs. For experiment ②, we attempt to test if METAEMU can run the firmware from its entry-point, allow it to perform peripheral initialization, and execute its main loop without crashing due to peripheral mishandling.

Discussion & results: For ①, we were able to trigger an out of bounds write with inputs exceeding a length of 62 bytes (the first two bytes of `i2cRxData` are populated using `i2c_device_info.addr` and `i2c_device_info.reg`) after only three iterations of our fuzz harness. This demonstrates that METAEMU is usable for analyzing firmware beyond our original use-case of automotive firmware, as well as its suitability for fuzz testing.

For ②, the author’s of P²IM [19] describe two *false* crashes/hangs induced by their framework when rehosting the Soldering Iron firmware. The first is caused by misclassification of a peripheral register, and the second is due to P²IM missing support for DMA-based peripherals. As METAEMU can support peripherals generically, we were able to rehost this firmware by intercepting DMA interactions by the firmware’s HAL interface in a manner similar to past work by Clements et al. [10]. We thus avoid the false crashes experienced by P²IM and μ Emu [61]. Since METAEMU provides an API to intercept any memory read/write (i.e., `hook_memory_write/read`), it can be extended to provide DMA support similar to DICE [37]. We note that since the author’s of P²IM do not provide source code for this firmware¹, we manually stubbed out the functionality relating to AFL, as it is unnecessary for our experiment.

6 HUMAN EFFORT

In this section, we discuss the human effort involved in using METAEMU for rehosting. As with any kind of reverse engineering, rehosting necessarily requires manual intervention for tasks that cannot be automated—from implementing complex peripherals to identifying functions to hook and override. METAEMU attempts to reduce this manual effort by moving towards a specification-based approach from one that is purely programmatic. In Table 1, we show the human effort involved in each of our case studies in terms of lines of code—all require under 1kloc—even in the case of complex inter-device analysis. Concretely, each case study took the author’s less than a day to implement.

The advantage of using our approach is twofold: firstly, a specification-based approach provides a DSL which enables much faster iteration of manual tasks such as implementing missing ISA instructions or peripheral models. As we separate specification files from the implementation of our tool, we can prototype new features without recompiling the tool, something not possible with QEMU-based rehosting approaches. Secondly, by using the same ISA specification language as Ghidra, we benefit from the maintenance and testing efforts of a large and active community. Ghidra’s repository contains specifications for 28 architectures and when

combined with community projects [16], METAEMU can rehost most ECUs without the need to implement any architectural support.

7 LIMITATIONS

In this section, we provide a discussion of METAEMU’s limitations. The correctness of METAEMU’s lifter depends on the processor definitions it uses as input. Fortunately, as they are based on Ghidra’s language definitions, we benefit from Ghidra’s large and active community that regularly contributes fixes.

The three peripheral interfaces in METAEMU provide a simple way to implement peripherals for automotive microcontrollers of atypical architectures, however, we have less peripheral models for common microcontrollers such as ARM or MIPS based devices. This makes it difficult to produce a direct comparison with existing emulators such as QEMU. As future work, we intend to explore adding a compatibility layer to allow METAEMU to use QEMU-derived peripheral models to address this issue, however, it would require implementing QEMU’s Object Model, memory, sysbus, interrupt, and peripheral APIs in METAEMU to do so. Our universal peripheral backend (§4.4.2) does not fully support Direct Memory Access (DMA)-based I/O, except when firmware interfaces with it using a HAL. Support for peripherals requiring this, however, can easily be added using METAEMU’s execution observers (§4.3).

While METAEMU’s runtime performance is comparable to Unicorn, there are possibilities for improvement, such as adding a JIT compiler for our IL. We believe such an enhancement will lead to even greater performance for our specification-based approach. However, it is unclear how to generically implement a JIT compiler that supports all of METAEMU’s different execution modes (§4.2.1).

8 DISCUSSION & RELATED WORK

Approaches to firmware rehosting cover a broad spectrum: in terms of the kind of analyses they facilitate, the degree to which they rely on hardware, the kinds of device they support, and the fidelity and faithfulness of the environments they transplant firmware into.

AVATAR [40, 58] and SURROGATES [32] propose hardware-in-the-loop analysis, which enables a device to be analyzed without handling many of the complexities of its peripherals. It permits a kind of hybrid methodology where a fast host can emulate most of the firmware and rely on the real device for peripheral I/O and interrupt handling. Many techniques have capitalized on these seminal works; for instance, Ruge et al. [48] use a hardware-in-the-loop approach to fuzz for vulnerabilities in bluetooth chips, while Gustafson et al. [24] use such an approach as a basis for their tool, Pretender, which automatically infers peripheral models from execution traces and device I/O behavior. INCEPTION [11] and HARD SNAP [12] use a hardware-in-the-loop approach for their debugger component; both attempt to handle the nuances of complex firmware and devices with multiple peripherals under symbolic execution.

In contrast to hardware-dependent approaches, emulation-based approaches do away with hardware interaction altogether, and to varying degrees attempt to emulate a device and its peripherals. Of the approaches that make their implementations open-source, we observe that almost all rely on either QEMU (e.g., [25]) or Unicorn (e.g., [36]) as the basis for their VXE. Clements et al. [10] emulate peripherals by hooking HAL APIs provided by many vendor SDKs.

¹https://github.com/RiS3-Lab/p2im-real_firmware/issues/2

They simulate peripheral interactions through generalized models that receive input and supply output via the hooked HAL functions. In [9] they extend their approach to support VxWorks-based devices. Feng et al. [19] rehost firmware to facilitate fuzz testing. To handle peripherals, they learn appropriate values for MMIO peripheral interactions based on device-specific *abstract peripheral models*. Mera et al. [37] propose a method to handle DMA-based peripheral inputs, similarly targeted at fuzzing rehosted firmware. Liu et al. [34] use model-guided execution to generate QEMU peripheral models from kernel device-tree and source code. Cao et al. [5], Johnson et al. [29], and Zhou [61], all leverage symbolic execution to learn *satisfying* values to bypass peripheral checks. Hernandez et al. [27] achieve full-system emulation of closed-source Shannon baseband firmware by adding missing architectural and peripheral support in QEMU, they later demonstrate that such an approach can be extended to other basebands [26]. In contrast to the aforementioned approaches, Milburn et al. [38] build a custom emulator and peripheral models to rehost an automotive instrument cluster; they use their emulator to aid in reverse-engineering the firmware’s UDS commands. Meanwhile, Davidson et al. [13] use full-system symbolic execution to discover vulnerabilities in PIC32 devices; they propose using specifications to configure interrupt and peripheral memory mappings, allowing their approach to be adapted to analyze different device configurations.

While pure emulation and hardware-in-the-loop approaches can achieve near complete support for a given device or family of devices, when based on commodity emulators, they are difficult to adapt to support devices based on esoteric architectures, such as automotive components, due to the substantial engineering effort required. Mera et al. [37] highlight this difficulty in their evaluation—to test their approach on both ARM and MIPS32-based devices, they need to build separate prototypes of their tool for two different forks of QEMU, as neither variant supports both architectures. Hernandez et al. [26] note the current impossibility of porting their baseband rehosting framework to work with Qualcomm basebands, due to lack of architecture support in the PANDA [15] QEMU fork.

As discussed in our evaluation, Ghidra provides a P-Code-based emulator, which can facilitate basic analysis tasks, including instruction hooking and manipulation of memory and register values. However, it lacks more advanced features for firmware reverse engineering, such as symbolic execution, and peripheral support. Although it is possible to add such functionality using its hooking API, its emulation performance is insufficient to support intensive tasks, such as fuzzing. Further, adding functionality to support dynamic changes to addressing modes, e.g., to correctly emulate C166-based firmware, would require extensive changes to the core of Ghidra’s emulator framework—a significant engineering task.

We provide a comparison of METAEMU with the state-of-the-art, using the framework classification proposed by Fasano [17] in Appendix G. The key difference between METAEMU and the frameworks listed, is that our approach generically enables analysis of firmware not currently supported by other frameworks with little effort. Moreover, like AVATAR, it is a general framework to build analysis tools, as opposed to a method to enable a specific type of analysis, e.g., fuzzing. As demonstrated through our case studies (§5.2), we can use METAEMU to build analyses similar to those proposed by other approaches (e.g., [5, 29]) in a completely

architecture-independent way, without resorting to implementing those techniques for many different emulators, or limiting the approach to a few architectures. As with other rehosting approaches, such as P²IM, METAEMU’s peripheral support will lead to better coverage when performing analysis tasks, such as fuzzing.

9 CONCLUSION

To conclude, we have presented the first architecture-agnostic framework capable of rehosting multiple devices simultaneously. Our IR lifter and simulators provide fully generic, extensible, architecture support, and our universal peripheral models and peripheral solver enable simulation of realistic execution environments. We also have tight integration with binary analysis tools to help manual analysis. Through our case studies, we have demonstrated that our tool is flexible, efficient, and can drive the analysis of real-world automotive firmware whose architectures are not supported by existing state-of-the-art rehosting approaches.

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APPENDICES

Due to space limitations, we provide appendices in the referenced supplementary material [8].

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