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Highly Integrated PA-PIFA With A Wide Frequency Tuning Range

Minyong Huang, Yunlong Lu, Qi-Ang Zhu, Milan Salek, Yi Wang, *Senior Member, IEEE*, Jifu Huang, and Taijun Liu, *Senior Member, IEEE*

***Abstract*— This letter presents a highly integrated power amplifier (PA)-antenna with capability of frequency tuning. A planar inverted-F antenna (PIFA) is used to directly match the PA transistor. This mitigates the lossy output matching network (OMN) in the PA-integrated antenna (PAIA). In order to achieve a wide frequency tuning range, a combination of capacitors are loaded at the PIFA to control the antenna input impedances, so that matching can be maintained with frequency tuning. The antenna analysis and design procedure of the tunable PAIA are detailed. For verification, a prototype is designed, fabricated and measured. Experimental results show that the frequency tuning range of the proposed PAIA covers from 2 to 4 GHz. Over this frequency tuning range, the effective isotropic radiation power (EIRP) and power-added efficiency (PAE) are higher than 40.5 dBm and 60% at the input power of 26.5 dBm, respectively.**

***Index Terms*—Active integrated antennas, output impedance matching network elimination, tunable, PIFA.**

I. Introduction

Power amplifier integrated antenna (PAIA) has advantages of compact size, low-cost and improved performances. This has gathered a lot of attention in applications of radar, imaging, and wireless power supply [1]-[3]. In order to improve the frequency agility of these applications and reduce the system circuit complexity, a frequency-tunable PAIA is highly desired. For example, when wirelessly powering sensors operating at different frequencies, the transmitter (power amplifier and antenna) is required to have the capability of frequency reconfiguration [4]-[6].

Conventional, PAIA is achieved by closely cascading the power amplifiers (PAs) and antennas (after matching to 50 Ω separately) or designing an impedance transformer network to match PA antenna [7]-[12]. However, these methods cannot eliminate the passive impedance matching network, which still restricts the size reduction and performance improvement, in terms of loss and parasitic radiation elimination. Recently, a new concept of unified and integrated circuit antenna (UNICA) was proposed in [13]. It aimed to achieve the seamless integration of circuit and antenna by eliminating the passive networks such as the matching networks and inter-connections. Some work has been published exploring this method. D-band amplifier-integrated antenna and arrays were designed and demonstrated in [14] by using 65-nm CMOS process. A power enhancement of 3.4 / 6 dB for a single element or a 2 × 2 layout was obtained. A transistor-integrated antenna as active frequency multiplier was presented in [15]. The output matching network (OMN) of transistor was replaced by the patch antenna to achieve compact size and high conversion gain. [16] presented a seamless integrated class-F PAIA. Compared with the conventional cascaded design of a PA and an antenna, the insertion loss was reduced by 0.95 dB and the corresponding power-add efficiency (PAE) was improved by 14.2%. A K-band slot antenna integrated with a GaN PA was shown in [17]. It achieved a total efficiency of 40% and an active gain of 15 dBi. In addition, a Doherty PA and a planar invert-F antenna (PIFA) were integrated and presented in [18]. The dual functions of impedance matching and active load modulation in Doherty PA were moved into the antenna to realize a high-density integration. However, all the previous work operate at a fixed frequency. It remains a challenge to design frequency tunable PAIA that eliminates impedance matching network to realize high PAE over a wide tunable frequency range.

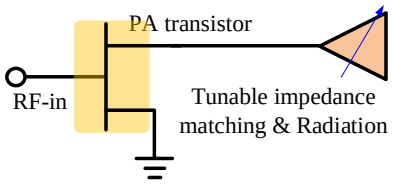

Fig. 1. Schematic of the seamlessly integrated frequency tunable PAIA.

This letter presents a highly integrated PAIA with a wide frequency tuning range. A tunable PIFA is used to directly match the output load impedance of the PA transistor at different frequencies. The tunable OMN in the conventional design can be eliminated. This helps to achieve a more compact PAIA with a consistently high PAE over a wide frequency tuning range.

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M. Huang, Y. Lu, Q.-A. Zhu, J. Huang, and T. Liu are with the Faculty of Electrical Engineering and Computer Science, Ningbo University, Ningbo, Zhejiang, 315211, China (e-mail: huangminyong8@163.com, luyunlong@nbu.edu.cn, huangjifu@nbu.edu.cn).

M. Salek, Y. Wang are with School of Engineering, University of Birmingham, B15 2TT, United Kingdom (e-mail: y.wang.1@bham.ac.uk).

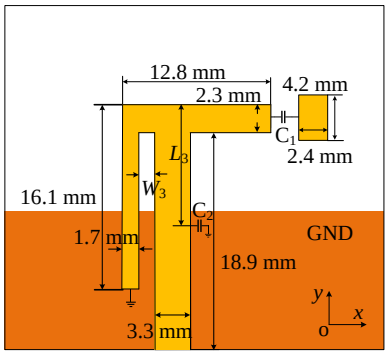

Fig. 2. Configuration of the proposed reconfigurable PIFA.

TABLE I
OPTIMAL LOAD IMPEDANCES BY LOAD PULL SIMULATION.

Freq (GHz)	For maximum P_{out} (Ω)	For maximum PAE (Ω)
2	3.15+j4.23	3.06+j10.07
2.5	4.22+j2.66	3.92+j8.04
3	6.24+j8.14	4.87+j7.52
3.5	8.43+j5.15	6.52+j3.76
4	10.23-j4.08	7.06-j3.42

II. DESIGN PROCEDURE

Fig. 1 shows the schematic of the seamless integrated tunable PAIA. The input impedance of the antenna at different frequencies is controlled to directly match the output impedance of the PA transistor. In this case, the antenna serves as a tunable OMN and a radiation element at the same time. Thus, a separate tunable matching network at the output of the PA transistor is no longer required. The proposed tunable PAIA is more compact and efficient. The design procedure is as follows:

(1) According to the desired output power level, efficiency and tunable frequency range, select the PA transistor and design the DC bias and stabilization circuits;

(2) Perform source-load pull analysis to obtain the input and output impedances of the PA transistor at different operating frequencies, considering the output power and efficiency requirements;

(3) Select an antenna and control its input impedance at the initial frequency (before frequency tuning) to match the output impedance of the PA transistor;

(4) Change the operating frequency, and design the input impedance of the antenna to match the output impedance of the PA transistor over the tunable frequency range;

(5) Design the wideband or tunable IMN of the PA transistor and connect the antenna.

III. DESIGN OF SEAMLESSLY INTEGRATED TUNABLE PAIA

A. PA transistor source-load pull analysis

Following the design procedure, the GaN HEMT CGH40010F transistor from Wolfspeed Inc. firstly selected as the power component. The transistor operates at Class-AB state with DC bias condition of V_{DS} = 28 V and V_{GS} = −2.8V. Then, the load-pull analysis for the PA transistor with bias and stabilization circuits at an input RF power of 26.5 dBm is simulated to obtain the load impedance characteristics. The results are given in Table I.

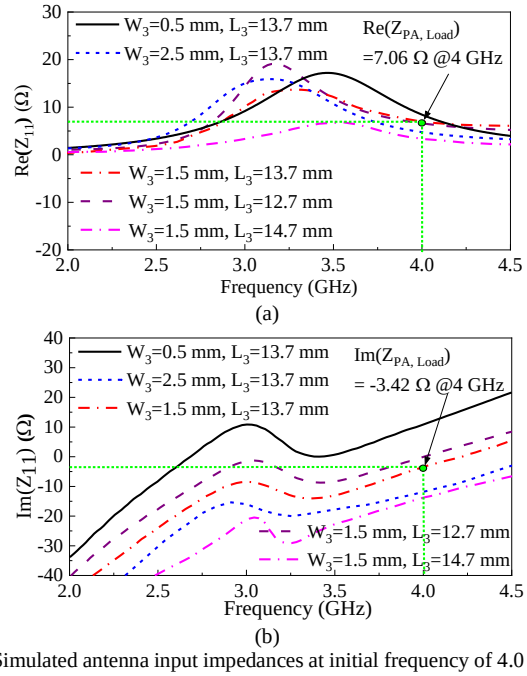

Fig. 3. Simulated antenna input impedances at initial frequency of 4.0 GHz. (a) Real and (b) imaginary parts.

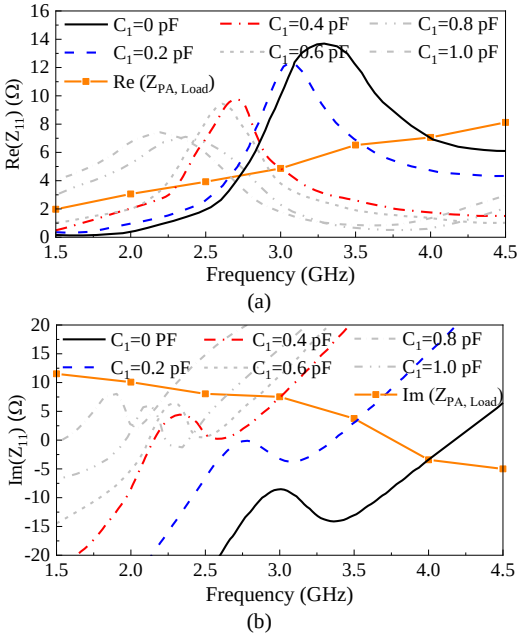

Fig. 4. Simulated antenna input impedances with varying capacitor C_1 (C_2 is fixed to 0.5 pF when $C_1 \neq$ 0 pF). (a) Real and (b) imaginary parts.

The load impedances at maximum PAE are preferred to achieve a high efficiency PIFA. In this case, the RF output power back-off is within ($P_{out,\ max}$ -1.5 dB) circle over the frequency range of 2 - 4 GHz. Subsequently, as described in design steps (3)-(5), an antenna is then designed so that its input impedances at different frequencies directly match the PA transistor.

B. Antenna analysis and design

The PIFA is selected to realize the integration with the PA transistor. The PIFA antenna is shown in Fig. 2. Rogers R4350B substrate with ε_r = 3.48, tanδ = 0.002 and a thickness of

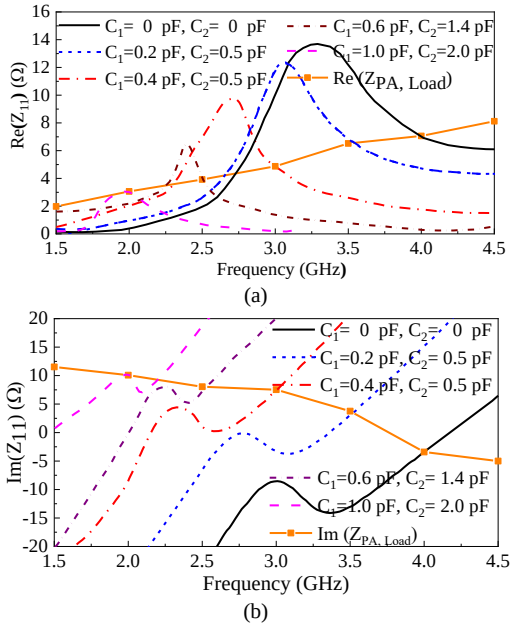

Fig. 5. Simulated antenna input impedances with varying capacitors C_1 and C_2. (a) Real and (b) imaginary parts.

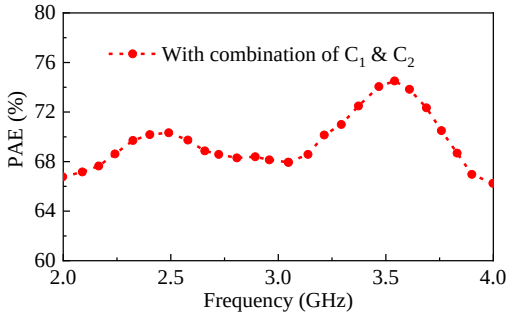

Fig. 6. Simulated PAE at different frequencies.

0.762 mm is used. Compared with an electrically small antenna, it is easier to control the real and imaginary parts of the impedance, and has a higher radiation efficiency. The capacitors are loaded to tunable the operating frequency of the PIFA. As mentioned above, the input impedance of the PIFA should be matched to the PA transistor over the frequency tuning range.For this purpose, the parameters of the PIFA are firstly optimized to satisfy the impedance requirement at the initial frequency (without the loaded capacitors) of 4 GHz. This is mainly controlled by the parameters W_3 and L_3. A parameter analysis is shown in Fig. 3. The dimensions are illustrated in Fig. 2. It can be seen from Fig. 3 that the input impedance of the PIFA at 4 GHz is matched with the PA transistor when W_3=1.5 mm and L_3=13.7 mm.

The combination of capacitors C_1 and C_2 is further employed to alter the operating frequency. Capacitor C_1 is attached to the radiation stub. By adjusting its value, the equivalent electrical length of the PIFA can be changed, thereby tuning the operating frequency. Fig. 4 shows the real and imaginary parts of the input impedance at different values of C_1, as well as the desired load impedances of PA transistor. When C_1 varies from 0 to 1 pF(C_2 is fixed to 0.5 pF when $C_1 \neq 0$ pF), the resonant frequency of PIFA is shifted from 4 to 2.17 GHz. However, the antenna

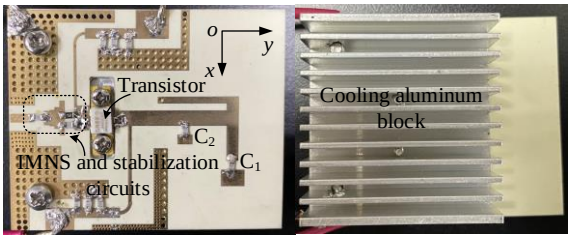

Fig. 7. Photograph of the seamlessly integrated tunable PAIA.

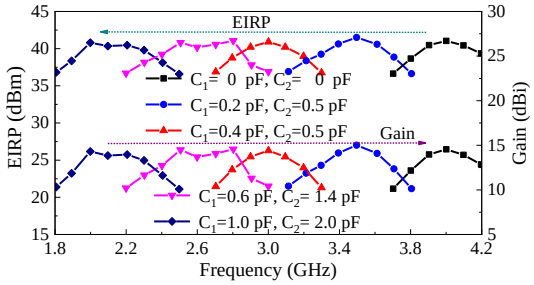

Fig. 8. Measured EIRP and gain at an input power of 26.5 dBm.

impedances only match the PA transistor in the range of 0 to 0.4 pF (corresponding to 3 - 4 GHz).Beyond this range, the antenna impedance starts to deviate from the desired load impedance of the PA transistor.

By changing its value, the frequency tuning range can be further expanded. Fig. 5 illustrates the antenna impedances at various combinations of C_1 and C_2. The real and imaginary parts of the antenna input impedance is re-aligned to the impedance requirement of PA transistor, when the operating frequency is lower than 3 GHz. As a result, the frequency tuning range is extended to 2 - 4 GHz while maintaining impedance matching between the antenna and the PA transistor. In addition, the simulated antenna radiation efficiency is higher than 95% at different frequencies, which ensures the overall high efficiency after the integration with the PA transistor. Fig. 6 shows the simulated power-added efficiency (PAE) of the PAIA. With the combination of C_1 and C_2, the PAE is maintained above 65% over the whole frequency tuning range of 2-4 GHz.

IV. Experimental Results

For demonstration, a prototype is designed and fabricated using the same substrate as the PIFA. The photograph of the prototype is shown in Fig. 7. It has a compact size of 44.2 mm × 54.5 mm. A wideband input impedance transformer network is used to match the input RF signal. The performance of the PAIA is tested in a microwave chamber with a pre-amplifier to increase the input RF signal power to the desired level, following the test procedure in [16], [17].

Fig. 8 shows the measured EIRP and active gain of the proposed PAIA. The operating frequency can be tuned from 4 to 2 GHz with different combination of capacitors C_1 and C_2, while the maximum EIRP maintains at over 40.5 dBm. For each operating state (fixed C_1 and C_2), the 1-dB bandwidth is about 350 MHz. After subtracting the RF input signal power (26.5 dBm), the maximum active gain of the PAIA is above 14.5 dBi over the entire frequency tuning range.

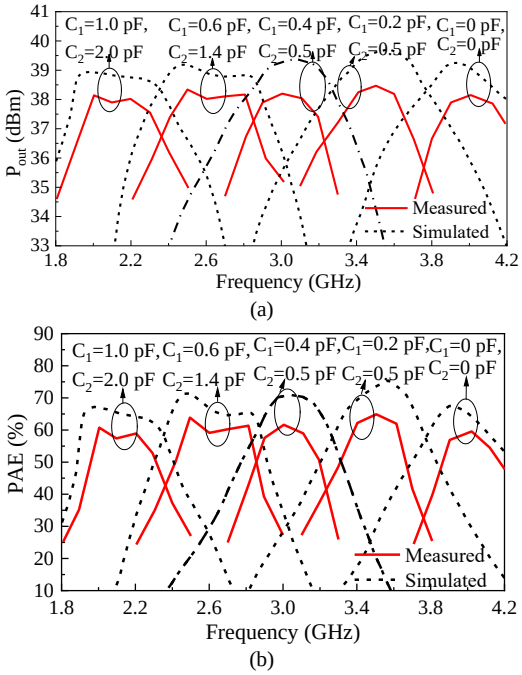

Fig. 9. Measured PAE and output power of the proposed PAIA at different frequencies. (a) P_{out}; (b) PAE.

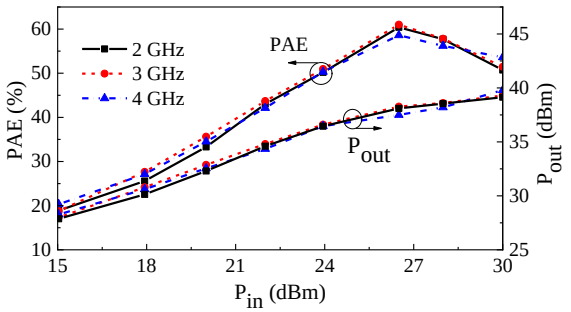

Fig. 10. Measured PAE and output power versus input power at different frequencies.

To calculate the measured output RF power (P_{out}) and PAE of the PAIA, we need to know the gain of PIFA. However, as the PIFA is directly matched to the PA transistor, it is difficult to measure the antenna peak gain by using the standard antenna test system. Instead, here we have used the simulated antenna gain to evaluate the performance of the PAIA. This is carried out by using Ansoft HFSS. The excitation port impedance is set to the load impedance of PA transistor in the simulation. Fig. 9 illustrates the measured RF output power and the PAE at different combination of C_1 and C_2. P_{out} varies from 38 dBm to 38.5 dBm over the frequency tuning range, whereas the corresponding PAE changes between 60 - 65%. The simulated P_{out} and PAE are also shown in Fig. 9. The simulated P_{out} is from 39 dBm to 39.7 dBm and the simulated PAE is in the range of 68 - 75.4%. The main reasons for the difference between the simulated and measured results are the parasitic effects introduced by soldering, the accuracy of the transistor model, and the influence of the heat sink. Fig. 10 shows the measured output RF power and PAE with increasing input power level at different operating frequencies. It can be seen

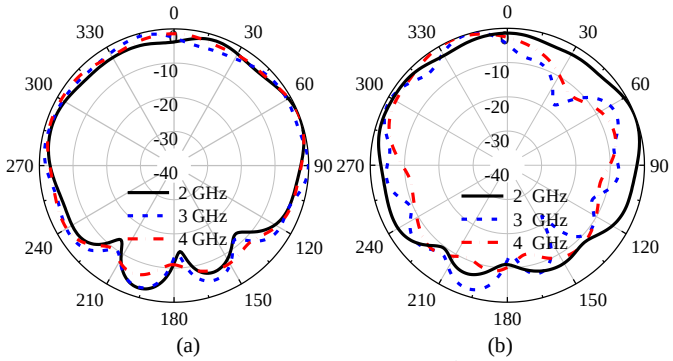

Fig. 11. Measured normalized radiation patterns of the proposed PAIA. (a) *xy*-plane, (b) *yz*-plane.

TABLE II
PERFORMANCE COMPARISON OF PA-IA

Ref.	Transistor	Freq (GHz)	EIRP (dBm)	PAE (%)	OMN	Tunable
[7]	GaAs	35	--	--	√	No
[12]	GaN	5.8	44.61	59.9	√	No
[14]	CMOS	146	-9.2	3.4	×	No
[16] Type I[1]	GaN	3.5	41.9	65.9	×	No
[16] Type II[2]		3.5	41.2	51.7	√	No
[17]	GaN	20	30.7	34.8	×	No
[18]	GaN	2.14	43.5	58	×	No
This work	GaN	2-4	>40.5	>60	×	Yes

[1]PAIA with direct matching
[2]PAIA with conventional design

that the peak PAEs at the three frequencies all appear at the input powers of 26.5 dBm. They are 61%, 63% and 60%, respectively. At this input power, the output powers are 38.2 dBm, 38.3 dBm and 38.1 dBm.

The measured normalized radiation patterns in *xy*- and *yz*-planes at 2, 3 and 4 GHz are plotted in Fig. 11. This measurement is performed at the input power of 26.5 dBm. The measured radiation patterns are slightly distorted from the standard PIFA due to the proximity of the active circuits and cooling aluminum block at the back side of the PA.

Table II compares this work with other PAIAs. Among them, the works in [7] and [12], as well as the type II in [16], have separate OMNs, and others are seamlessly integrated. The results in [16] show that PAIA employing direct matching can effectively reduce loss and enhance overall performance. However, all the previous works operate at a fixed frequency. None of them demonstrated the capability of frequency tuning. This design successfully realized the frequency tuning function, while keeping high PAE and power output.

V. CONCLUSION

This letter demonstrated a highly integrated PAIA with capability of wide frequency tuning. A PIFA with an initial operating frequency of 4 GHz is designed to match the PA transistor directly. With the assistance of two loaded capacitors in the PIFA, the proposed PAIA is capable of adjusting its operating frequency in a wide frequency range, while maintaining high EIRP and PAE. Experimental results validate the design concept. The proposed PAIA is a good candidate for future emerging active antenna applications.

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